Estd:1917

Prof. P. Chandra Sekhar

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Estd:1929

No.:1381 /Admn/UCE OU/ 2026 **Date: 17.11.2026**

Advertisement for Project Associate - I position in the MeitY sponsored Chips to Startup(C2S) Program in the Department of Electronics & Communication Engineering, University College of Engineering (A), Osmania University

Applications are invited from eligible candidates to work as JRF/Project Associate in C2S Project titled "The Design, Fabrication and Development of Silicon Proven IP Core for High Resolution ADPLL"

Aim of the Project: Aim of the project is to Design, Fabricate and Develop silicon proven, state of art, IP Core for high resolution All Digital Phase Locked Loop ADPLL suitable for Multipurpose Low Energy Applications.

For more information regarding the project, visit: http://www.uceou.edu/pdfs/faculty/50022-ADPLL-IP-Core-C2S-MeitTy.pdf

Number of positions available: ONE (1)

Qualification:

- Bachelor's degree in Electronics and Communication Engineering/ ME/ M.Tech. in Electronics and Communication Engineering /VLSI / or related area with first class.
- Preference will be given to candidates who are GATE/NET qualified and have experience in Verilog, Verilog-A, Analog and Digital ASIC Design (Cadence, Synopsys)

Fellowship:

- Rs. 37,000 per month + HRA as per norms (for project tenure of minimum One Year) for GATE/NET qualified candidates
- Rs. 31,000 per month + HRA as per norms (for project tenure of minimum One Year) for other candidates

General Term and Condition: The position is temporary and renewable each year subject to satisfactory performance. The position is co-terminus with the project. The age limit is 35 years (5 years' relaxation for SC/ST/OBC/ female/Physically Handicapped Candidate).

Completely filled, signed application form must be submitted as per the template provided (Annexure – I). Original documents of age proof/certificates/degrees/mark sheets and other testimonials must be presented at the time of interview. Attested photocopies of these documents will be collected at the time of interview. Only shortlisted candidates will be communicated through e-mail to appear in the interview and no other communications in this regard will be entertained.

No TA/DA will be paid for attending the interview.

Completed applications should reach **on or before 26th November, 2026** via email attachment addressed to:

Prof. P. Chandra Sekhar
Chief Investigator
sekharp@osmania.ac.in

PRINCIPAL

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83319 97292

ESTD: 1917

University College of Engineering

(AUTONOMOUS)

OSMANIA UNIVERSITY, HYDERABAD - 500 007.

ESTD: 1929

ANNEXURE- I

APPLICATION FORM FOR POST OF PROJECT ASSOCIATE- I IN THE MEITY SPONSORED CHIP TO STARTUP (C2S) PROGRAM IN THE DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

1. Name in full (in BLOCK letters):

Paste a recent passport size photograph

2. Parent's Name:

3. Date of birth :

4. Present address for correspondence:

Mobile:
Email ID:

5. GATE/CSIR/UGC Exam : Y/N
(If Yes then give the percentage mark/rank and year of passing)

6. Educational Qualifications: (From SSC) (add more rows as required)

Sl. No	Qualification	Board/University	Year of passing	Percentage (%)

7. Experience:

Name of Post	Name of Organisation /Dept.	From	To	Nature of duties performed

8. Number of Publications in Journals / Conferences*:

9. Courses/Training in VLSI(provide proof):

DECLARATION

I hereby, undertake that all the details furnished above are true to the best of my knowledge and I am liable for any disciplinary action, if found otherwise. My candidature may kindly be considered for the above temporary/contractual/short-term project position as per the rules of UGC/DST/MietY.

Place:
Date: Signature

INSTRUCTIONS:

1. The application form should be neatly typed and sent by e-mail (sekharp@osmania.ac.in) so as to reach before the deadline i.e 26-11-2026.
2. *Enclose photo copies of certificates and reprints of published work.